Amendments to the Claims

1. (Currently Amended) ~~Testing device~~ A testing device for testing a phase locked loop having a power supply input, said testing device comprising:

[[-]] a power supply unit for providing a power supply signal ~~(VDD)~~ having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal ~~(Uout)~~

[[-]] a means for disabling a feedback signal to a phase comparator of the phase locked loop such that said phase locked loop is operated in an open loop mode, and

[[-]] a meter for measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input.

2. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device according to claim 1, said phase locked loop (PLL) having phase comparator ~~(10)~~ and said phase comparator (10) having a feedback input ~~(Ufb)~~ and a reference input ~~(Uref)~~, wherein

[[-]] both said feedback input (Uth) and said reference input (Uref) are connected to ground.

3. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device ~~according to claims 1 or 2~~, according to claim 1, comprising a periodic signal generator for providing a periodic input signal having the same frequency to said feedback input ~~(Ufb)~~ and to said reference input ~~(Uref)~~.

4. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device ~~according to claims 1, 2 or 3,~~ according to claim 1, wherein said meter is adapted to measure a current (IDD) provided to at least one of the following: the power supply input, an output voltage an output voltage, ~~(Uout) and/or~~ an oscillator control voltage ~~(UVCO)~~ of the phase locked loop.

5. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device ~~according to claim 1, 2, 3 or 4,~~ according to claim 1, wherein said power supply unit is adapted to provide a periodic power supply signal ~~(Vdd)~~.

6. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device ~~according to claims 1, 2, 3, 4 or 5,~~ according to claim1, wherein the power supply unit and the periodic signal generator are both adapted to provide periodic signals having the same frequency.

7. (*Currently Amended*) ~~Testing device~~ The testing device for testing a phase locked loop device according to one of claims 1 to 6, according to claim 1, wherein the power supply unit and the periodic signal generator are both adapted to provide periodic signals having a phase difference between the periodic power supply signal (VDD) and the periodic input signal is equal to 0, T'/4 or 3T/4, T being a period of both said periodic power supply signal (VDD) and said periodic input signal.

8. (*Currently Amended*) ~~Testing device~~ The testing device according to claim 4, comprising

[[-]] a high pass filter for filtering the current (IDD) provided to the power supply input, and

[[-]] an integrator for integrating the filtered power supply current (IDD), wherein the integrated power supply current is indicative of a defective phase locked loop.

9. (*Currently Amended*) ~~Phase locked loop comprising a testing device according to one of the preceding claims.~~ A phase locked loop comprising the testing device according to claim 1.

10. (*Currently Amended*) Method for testing a phase locked loop (PLL) having a power supply input, comprising the steps:

[[-]] operating the phase locked loop in an open loop mode

[[-]] providing a power supply signal ~~(VDD)~~ having a variation profile to the power supply input of the phase locked loop, wherein a width and height of said variation profile are formed in such a way, that the voltage controlled oscillator is prevented from outputting an oscillating output signal ~~(Uout)~~, and

[[-]] measuring a measurement signal of the phase locked loop, while said power supply signal is provided to the power supply input of the phase locked loop.

11. (*Currently Amended*) Method for testing a phase locked loop device (PLL-device) according to claim 10, wherein said variation profile of the power supply signal has a ascending edge, said ascending edge being short enough (T_{RISE}) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal ~~(Uout)~~.

12. (*Currently Amended*) Method for testing a phase locked loop device ~~according to claim 10 or 11,~~ according to claim 10, wherein said variation profile of the power supply signal has a descending edge, said descending edge being short enough (T) to prevent the voltage controlled oscillator (VCO) from outputting an oscillating output signal (Uoui).

13. (*Currently Amended*) Method for testing a phase locked loop device ~~according to claim 10, 11 or 12,~~ according to claim 10, said phase locked loop (PLL) having phase comparator ~~(10)~~ and said phase comparator (10) having a feedback input (Ufb) and a reference input (Uref), wherein

- both said feedback input (Utb) and said reference input (Uref) are connected to ground.

14. (*Currently Amended*) Method for testing a phase locked loop device ~~according to claim 10, 11 or 12,~~ according to claim 10, wherein said feedback input ~~(Ufb)~~ and said reference input ~~(Uref)~~ receive an identical periodic input signal.

15. (*Currently Amended*) Method for testing a phase locked loop device according ~~to one of the preceding claims~~to claim 10, wherein the measurement signal is a current ~~(IDD)~~ provided to the power supply input, an output voltage ~~(Uout)~~ and/or an oscillator control voltage ~~(Uvco)~~ of the phase locked loop.

16. (*Currently Amended*) Method for testing a phase locked loop device ~~according to one of the preceding claims,~~ according to claim 10, wherein the power supply signal ~~(VDD)~~ is a periodic voltage signal.

17. (*Currently Amended*) Method for testing a phase locked loop device ~~according to claims 15 and 16,~~ according to claim 15, wherein the periodic power supply signal ~~(VDD)~~ and the periodic input signal to the reference input ~~(Uref)~~ have the same frequency.

18. (*Currently Amended*) Method for testing a phase locked loop device according to claim 17, wherein a phase difference between the periodic power supply signal ~~(VDD)~~ and the periodic input signal is equal to 0, T/4 or 3T/4, T being a period of both said periodic power supply signal ~~(VDD)~~ and said periodic input signal.